LM2612BL 400mA Sub-miniature, Programmable, Step-Down DC-DC Converter for Ultra Low-Voltage Circuits

Check for Samples: LM2612BL

FEATURES

- **Sub-miniature 10-pin DSBGA Package**
- **Only Three Tiny Surface-mount External Components Required**
- **Uses Small Ceramic Capacitors**
- **Internal Soft Start**
- **Current Overload Protection**
- **No External Compensation Required**
- **Thermal Shutdown Protection**

KEY SPECIFICATIONS

- **Operates from a Single LiION Cell (2.8V to 5.5V)**
- **Internal Synchronous Rectification for High PWM Mode Efficiency**
- **Pin Programmable Output Voltage (1.05V, 1.3V, 1.5V and 1.8V)**
- **400mA Maximum Load Capability (300mA for B Grade)**
- **±2% PWM Mode DC Output Voltage Precision**
- **5mV typ PWM Mode Output Voltage Ripple**
- **160 µA typ PFM Mode Quiescent Current**
- **0.02µA typ Shutdown Mode Current**
- **600kHz PWM Mode Switching Frequency**
- **SYNC Input for PWM Mode Frequency Synchronization from 500kHz to 1MHz**

APPLICATIONS

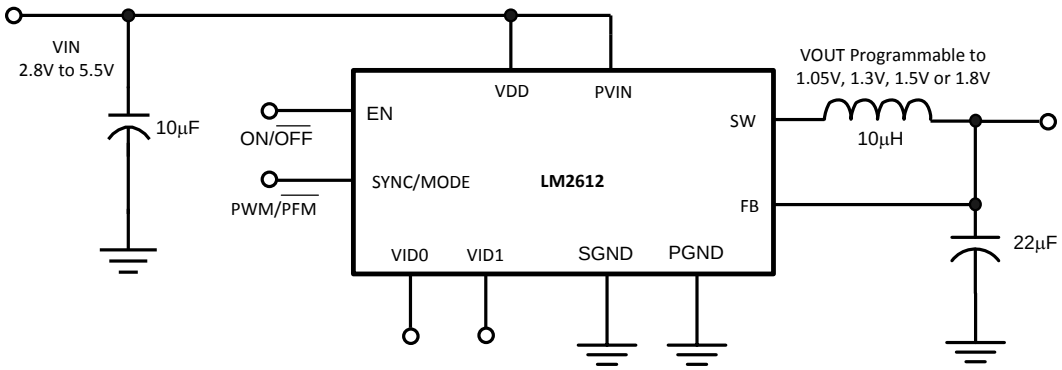
- **Mobile Phones**
- **Hand-Held Radios**
- **Battery Powered Devices**

DESCRIPTION

The LM2612 step-down DC-DC converter is optimized for powering ultra-low voltage circuits from a single Lithium-Ion cell. It provides up to 400mA (300mA for B grade), over an input voltage range of 2.8V to 5.5V. Pin programmable output voltages of 1.05V, 1.3V, 1.5V or 1.8V allow adjustment for MPU voltage options without board redesign or external feedback resistors.

The device has three pin-selectable modes for maximizing battery life in mobile phones and similar portable applications. Low-noise PWM mode offers 600kHz fixed-frequency operation to reduce interference in RF and data acquisition applications during full-power operation. In PWM mode, internal synchronous rectification provides high efficiency (91% typ. at $1.8V_{OUT}$). A SYNC input allows synchronizing the switching frequency in a range of 500kHz to 1MHz to avoid noise from intermodulation with system frequencies. Low-current hysteretic PFM mode reduces quiescent current to 160 µA (typ.) during system standby. Shutdown mode turns the device off and reduces battery consumption to 0.02µA (typ.). Additional features include soft start and current overload protection.

Typical Application Circuit



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DESCRIPTION (CONTINUED)

The LM2612 is available in a 10 pin DSBGA package. This package uses TI's wafer level chip-scale DSBGA technology and offers the smallest possible size. Only three small external surface-mount components, an inductor and two ceramic capacitors are required.

Connection Diagrams

DSBGA Package

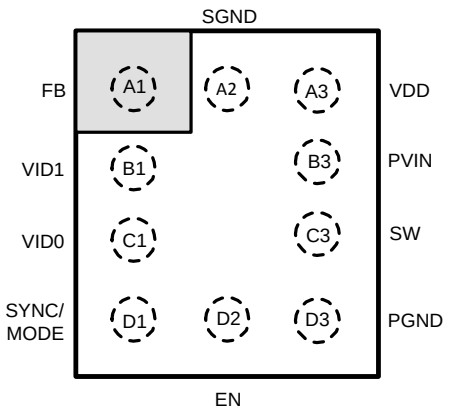

Figure 1. TOP VIEW

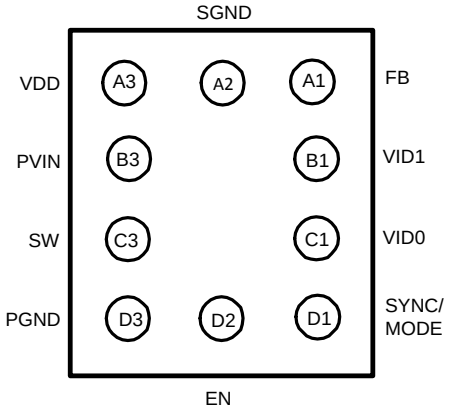

Figure 2. BOTTOM VIEW

PIN DESCRIPTION

Pin Number[(1)]	Pin Name	Function
A1	FB	Feedback Analog Input. Connect to the output at the output filter capacitor (Figure 1)
B1	VID1	Output Voltage Control Inputs. Set the output voltage using these digital inputs (see Table 1). The output defaults to 1.5V if these pins are unconnected.
C1	VID0	
D1	SYNC/MODE	Synchronization Input. Use this digital input for frequency synchronization or modulation control. Set: SYNC/MODE = high for low-noise 600kHz PWM mode SYNC/MODE = low for low-current PFM mode SYNC/MODE = 500kHz - 1MHz external clock for synchronization to an external clock in PWM mode. See *Frequency Synchronization (SYNC/MODE Pin)* and *Operating Mode Selection (SYNC/MODE Pin)* in the DEVICE INFORMATION section.
D2	EN	Enable Input. For shutdown, set low to SGND.(See *Shutdown Mode* in the *DEVICE INFORMATION* section.)
D3	PGND	Power Ground
C3	SW	Switching Node connection to the internal PFET switch and NFET synchronous rectifier.
B3	PVIN	Power Supply Input to the internal PFET switch. Connect to the input filter capacitor (Figure 29).
A3	VDD	Analog Supply Input. If board layout is not optimum, an optional 0.1µF ceramic capacitor is suggested (Figure 29)
A2	SGND	Analog and Control Ground

(1) The pin numbering scheme for the DSBGA package was revised in April, 2002 to conform to JEDEC standard. Only the pin numbers were revised. No changes to the physical location of the inputs/outputs were made. For reference purpose, the obsolete numbering had FB as pin 1, VID1 as pin 2, VID0 as pin 3, SYNC as pin 4, EN as pin 5, PGND as pin 6, SW as pin 7, PVIN as pin 8, VDD as pin 9 and SGND as pin 10.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

PVIN, VDD, to SGND	−0.2V to +6V
PGND to SGND	−0.2V to +0.2V
EN, SYNC/MODE, VID0, VID1 to SGND	−0.2V to +6V
FB, SW	(GND −0.2V) to (VDD +0.2V)
Storage Temperature Range	−45°C to +150°C
Lead temperature (Soldering, 10 sec.)	260°C
Junction Temperature [3]	−25°C to 125°C
Minimum ESD Rating Human body model, C = 100pF, R = 1.5 kΩ	±2kV
Thermal Resistance (θ_{JA}) LM2612ABL/LM2612ATL & LM2612BBL/LM2612BTL[4]	140°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but parameter specifications may not be ensured. For ensured specifications and associated test conditions, see the Min and Max limits and Conditions in the Electrical Characteristics table. Electrical Characteristics table limits are specified by production testing, design or correlation using standard Statistical Quality Control methods. Typical (Typ) specifications are mean or average values from characterization at 25°C and are not ensured.
(2) **If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office / Distributors for availability and specifications.**
(3) Thermal shutdown will occur if the junction temperature exceeds the 150°C maximum junction temperature of the device.
(4) Thermal resistance specified with 2 layer PCB(0.5/0.5 oz. cu).

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for $T_A = T_J = 25°C$, and those in **bold face type** apply over the full Operating Temperature Range ($T_A = T_J = -25°C$ to +85°C). Unless otherwise specified, PVIN = VDD = EN = SYNC = 3.6V, VID0 = VID1 = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IN}	Input Voltage Range [1]	PVIN = VDD = VID1 = V_{IN}, VID0 = 0V	2.8		5.5	V
V_{FB}	Feedback Voltage [2]	VID0 = V_{IN}, VID1 = V_{IN}	**1.029**	1.05	**1.071**	V
		VID0 = V_{IN}, VID1 = 0V	**1.274**	1.30	**1.326**	
		VID0 = 0V, VID1 = 0V	**1.470**	1.50	**1.530**	
		VID0 = 0V, VID1 = V_{IN}	**1.764**	1.8	**1.836**	
V_{HYST}	PFM Comparator Hysteresis Voltage [3]	PFM Mode (SYNC = 0V)		25		mV
I_{SHDN}	Shutdown Supply Current	EN = 0V		0.02	**3**	µA
I_{Q1}	DC Bias Current into VDD	No switching, PFM mode (SYNC/MODE = 0V)		160	**195**	µA
I_{Q2}		No switching, PWM mode (SYNC/MODE = V_{IN})		605	**725**	
$R_{DSON\ (P)}$	Pin-Pin Resistance for P FET			395	550	mΩ
$R_{DSON\ (N)}$	Pin-Pin Resistance for N FET			325	500	mΩ
$R_{DSON\ ,\ TC}$	FET Resistance Temperature Coefficient			0.5		%/C

(1) The LM2612 is designed for applications where turn-on after system power-up is controlled by the system processor and internal UVLO (Under Voltage LockOut) circuitry is unnecessary. The LM2612 has no UVLO circuitry and should be kept in shutdown by holding the EN pin low until the input voltage exceeds 2.8V. Although the LM2612 exhibits safe behavior while enabled at low input voltages, this is not ensured.
(2) The feedback voltage is trimmed at the 1.5V output setting. The other output voltages result from the pin selection of the internal DAC's divider ratios. The precision for the feedback voltages is ±2%.
(3) The hysteresis voltage is the minimum voltage swing on FB that causes the internal feedback and control circuitry to turn the internal PFET switch on and then off during PFM mode.

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ELECTRICAL CHARACTERISTICS (continued)

Specifications with standard typeface are for $T_A = T_J = 25°C$, and those in **bold face type** apply over the full Operating Temperature Range ($T_A = T_J = -25°C$ to $+85°C$). Unless otherwise specified, PVIN = VDD = EN = SYNC = 3.6V, VID0 = VID1 = 0V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{lim}	Switch Peak Current Limit (4)	LM2612ABL/LM2612ATL	**510**	710	**850**	mA
		LM2612BBL/LM2612BTL	**400**	710	**980**	
V_{EN_H}	EN Positive Going Threshold Voltage			0.95	**1.3**	V
V_{EN_L}	EN Negative Going Threshold Voltage		**0.4**	0.80		V
V_{SYNC_H}	SYNC/MODE Positive Going Threshold Voltage			0.95	**1.3**	V
V_{SYNC_L}	SYNC/MODE Negative Going Threshold Voltage		**0.4**	0.84		V
V_{ID_H}	V_{ID0}, V_{ID1} Positive Going Threshold Voltage			0.92	**1.3**	V
V_{ID_L}	V_{ID0}, V_{ID1} Negative Going Threshold Voltage		**0.4**	0.83		V
I_{VID}	VID1, VID0 Pull Down Current	VID1, VID0 = 3.6V		1.8	**3.0**	µA
f_{sync}	SYNC/MODE Clock Frequency Range (5)		**500**		**1000**	kHz
F_{OSC}	Internal Oscillator Frequency	LM2612ABL/ATL, PWM Mode (SYNC = VIN)	468	600	732	kHz
		LM2612BBL/BTL, PWM Mode (SYNC = VIN)	450	600	750	
T_{min}	Minimum ON-Time of P FET Switch in PWM Mode			200		nS

(4) Current limit is built-in, fixed, and not adjustable. If the current limit is reached while the output is pulled below about 0.7V, the internal PFET switch turns off for 2.5 µs to allow the inductor current to diminish.
(5) SYNC driven with an external clock switching between V_{IN} and GND. When an external clock is present at SYNC, the IC is forced to PWM mode at the external clock frequency. The LM2612 synchronizes to the rising edge of the external clock.

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TYPICAL OPERATING CHARACTERISTICS

LM2612ABL/ATL, Circuit of Figure 29, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

Quiescent Supply Current vs Temperature

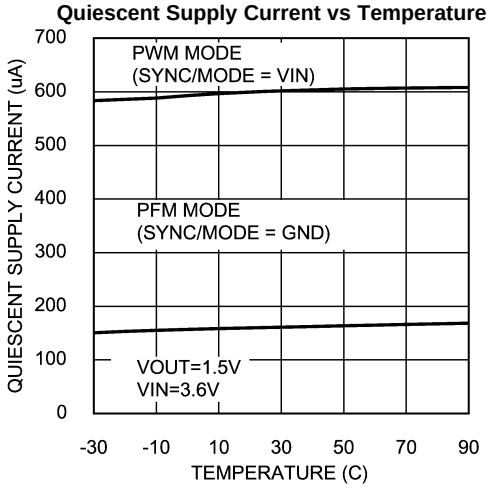

Figure 3.

Quiescent Supply Current vs Supply Voltage

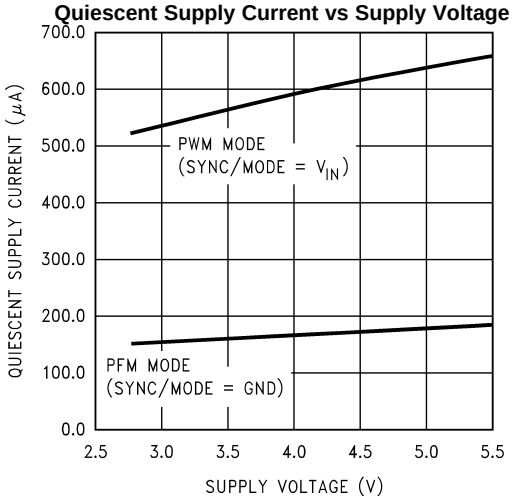

Figure 4.

Shutdown Quiescent Current vs Temperature

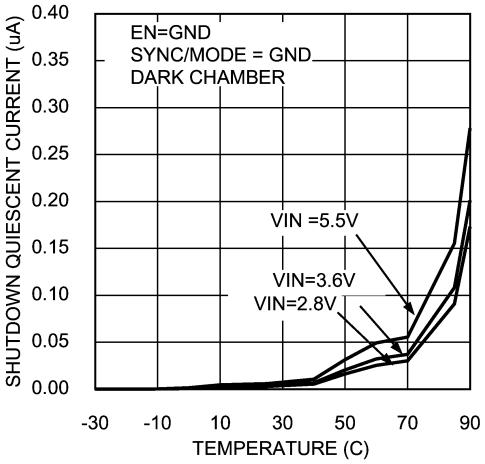

Figure 5.

Output Voltage vs Temperature (PWM Mode)

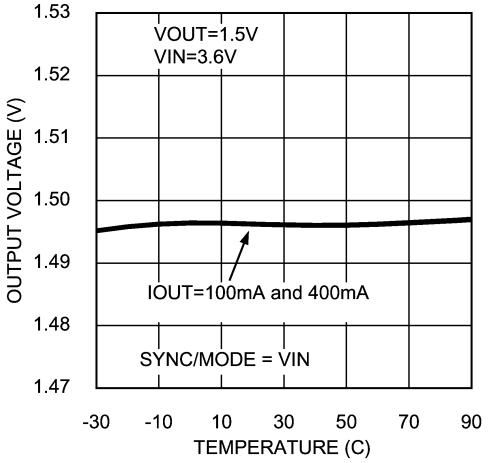

Figure 6.

Output Voltage vs Temperature (PFM Mode)

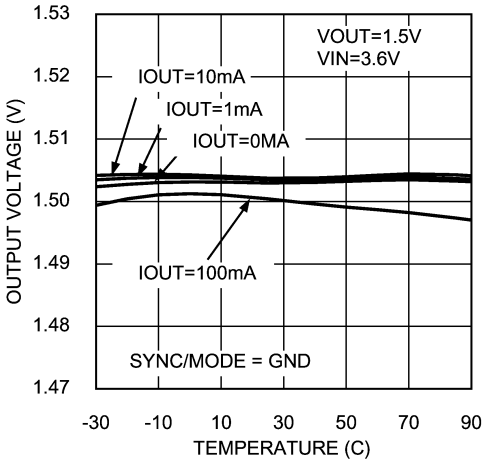

Figure 7.

Output Voltage vs Supply Voltage (V_{OUT} = 1.5V, PWM Mode)

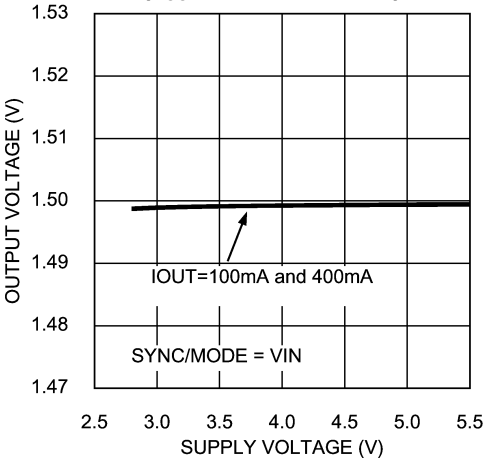

Figure 8.

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TYPICAL OPERATING CHARACTERISTICS (continued)

LM2612ABL/ATL, Circuit of Figure 29, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

Output Voltage vs Supply Voltage (V_{OUT} = 1.5V, PFM Mode)

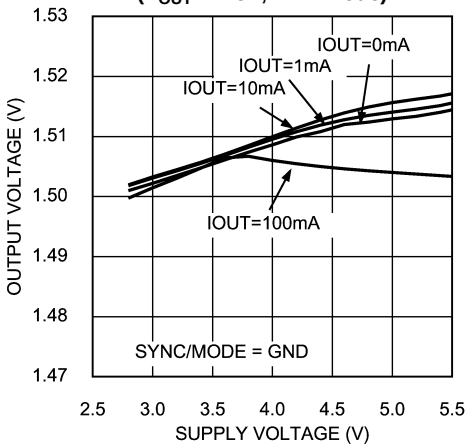

Figure 9.

Output Voltage vs Output Current (V_{OUT} = 1.5V, PWM Mode)

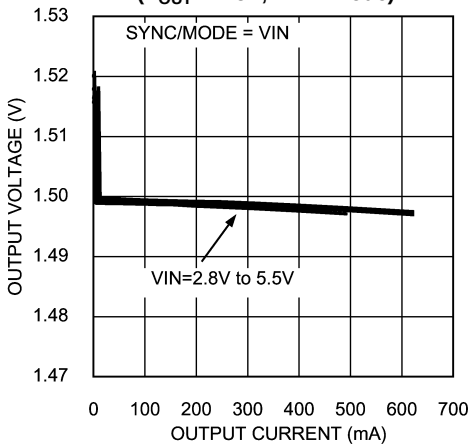

Figure 10.

Output Voltage vs Output Current (V_{OUT} = 1.5V, PFM Mode)

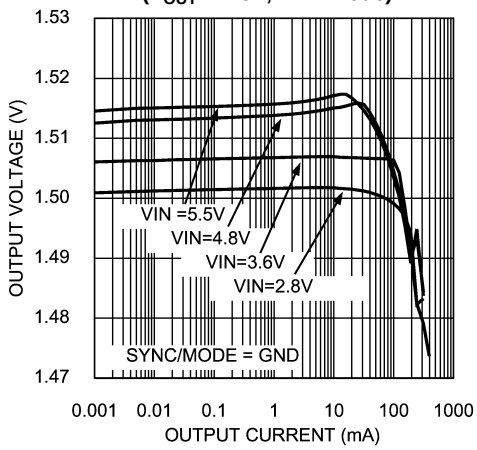

Figure 11.

Efficiency vs Output Current (V_{OUT} = 1.8V, PWM Mode, With Diode)

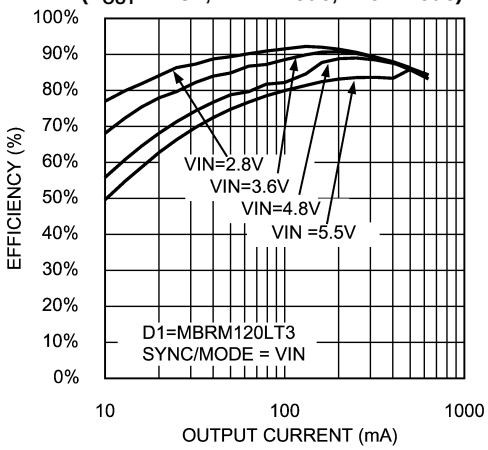

Figure 12.

Efficiency vs Output Current (V_{OUT} = 1.8V, PFM Mode, With Diode)

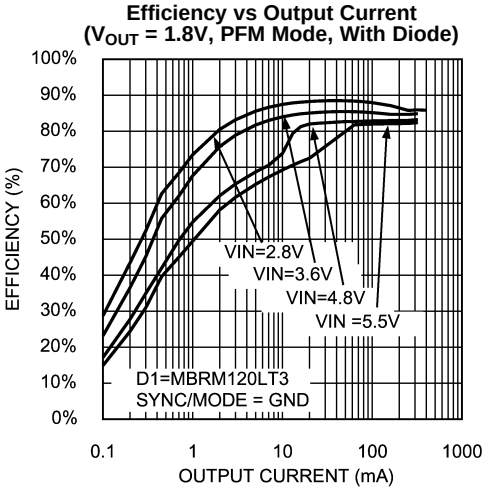

Figure 13.

Efficiency vs Output Current (V_{OUT} = 1.5V, PWM Mode, With Diode)

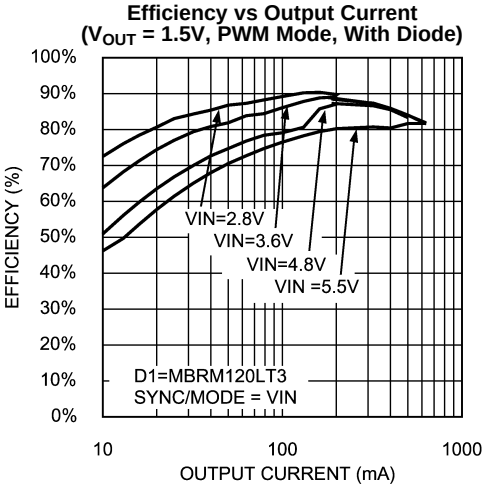

Figure 14.

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TYPICAL OPERATING CHARACTERISTICS (continued)

LM2612ABL/ATL, Circuit of Figure 29, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

Efficiency vs Output Current (V_{OUT} = 1.5V, PFM Mode, With Diode)

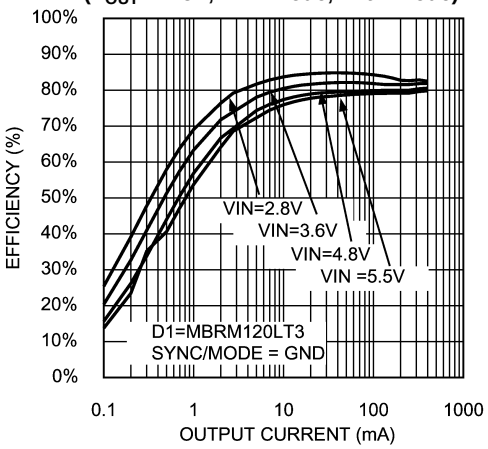


Figure 15.

Efficiency vs Output Current (V_{OUT} = 1.3V, PWM Mode, With Diode)

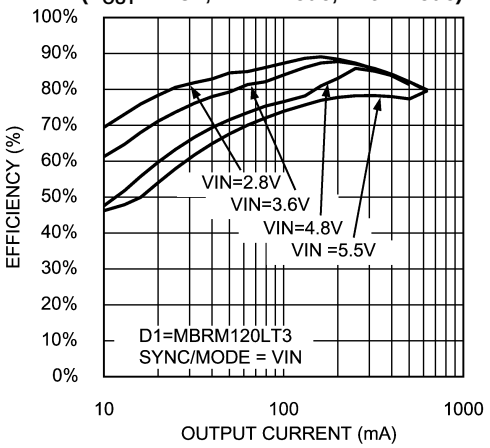


Figure 16.

Efficiency vs Output Current (V_{OUT} = 1.3V, PFM Mode, With Diode)

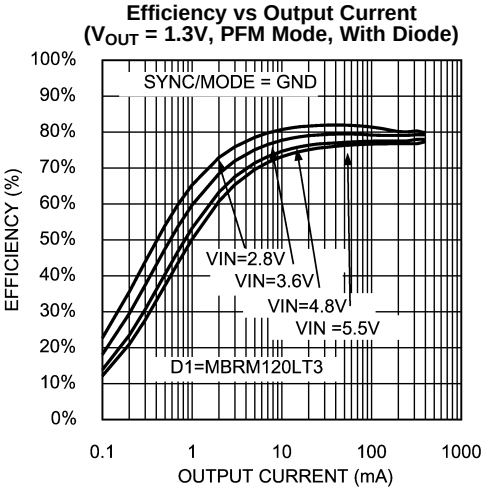


Figure 17.

Efficiency vs Output Current (V_{OUT} = 1.05V, PWM Mode, With Diode)

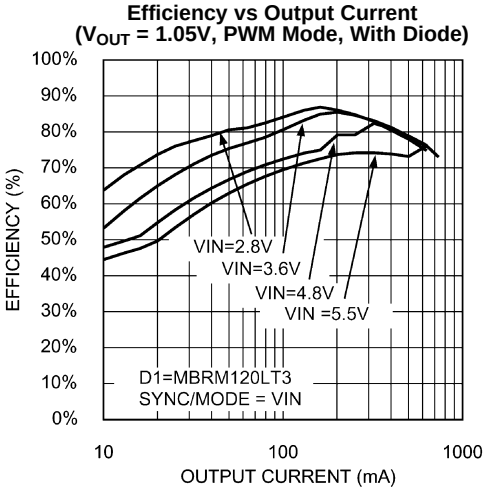


Figure 18.

Efficiency vs Output Current (V_{OUT} = 1.05V, PFM Mode, With Diode)

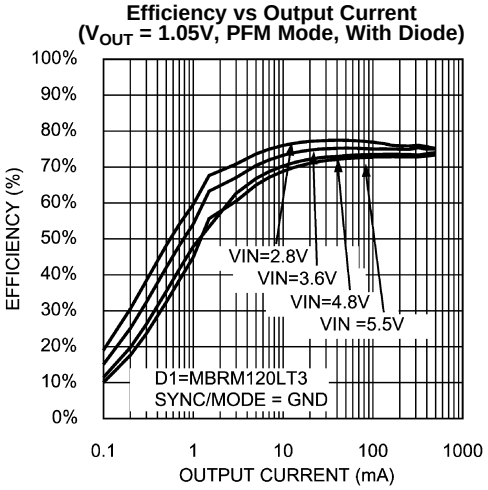


Figure 19.

Efficiency vs Output Current (V_{OUT} = 1.8V, PWM Mode,No Diode)

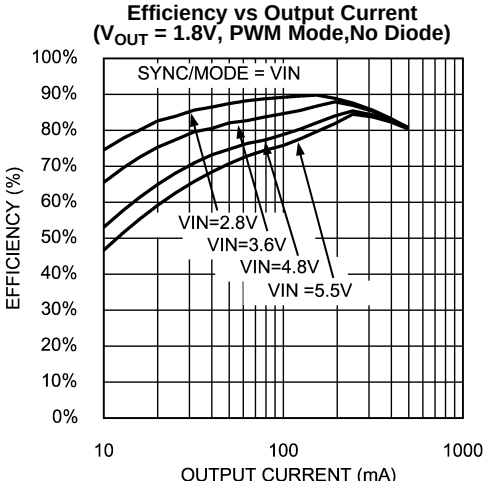


Figure 20.

TYPICAL OPERATING CHARACTERISTICS (continued)

LM2612ABL/ATL, Circuit of Figure 29, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

Efficiency vs Output Current (V_{OUT} = 1.8V, PFM Mode, No Diode)

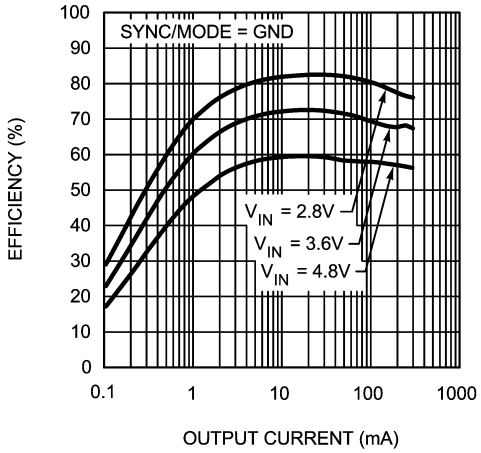


Figure 21.

Switching Frequency vs Temperature (PWM Mode)

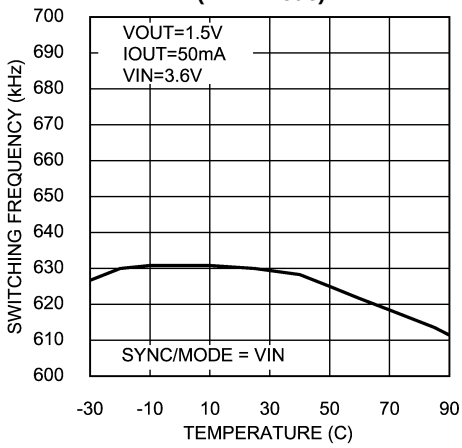
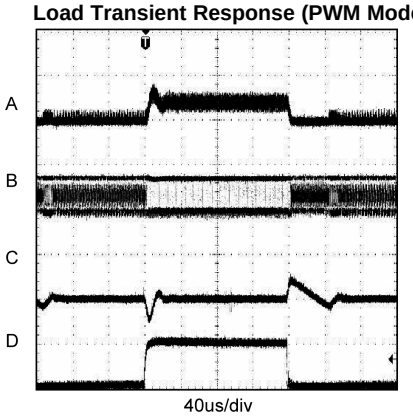


Figure 22.

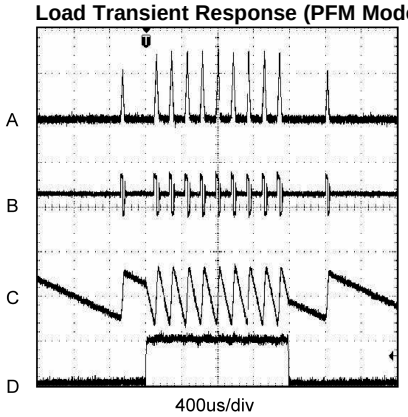
Load Transient Response (PWM Mode)



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 5V/div
C: V_{OUT}, 50mV/div, AC COUPLED
D: LOAD, 20mA to 200mA, 200mA/div

Figure 23.

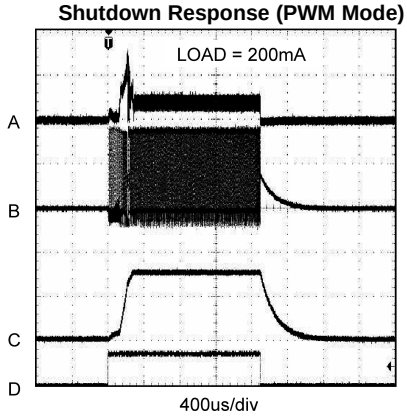
Load Transient Response (PFM Mode)



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 5V/div
C: V_{OUT}, 50mV/div, AC COUPLED,
D: LOAD, 10mA to 100mA, 100mA/div

Figure 24.

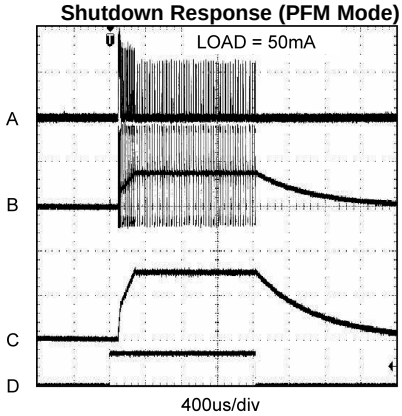
Shutdown Response (PWM Mode)



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 2V/div
C: V_{OUT}, 1V/div, D: EN, 5V/div

Figure 25.

Shutdown Response (PFM Mode)



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 2V/div
C: V_{OUT}, 1V/div , D: EN, 5V/div

Figure 26.

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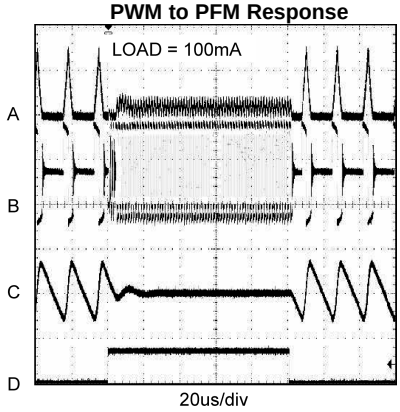
TYPICAL OPERATING CHARACTERISTICS (continued)

LM2612ABL/ATL, Circuit of Figure 29, V_{IN} = 3.6V, T_A = 25°C, L_1 = 10 µH, unless otherwise noted.

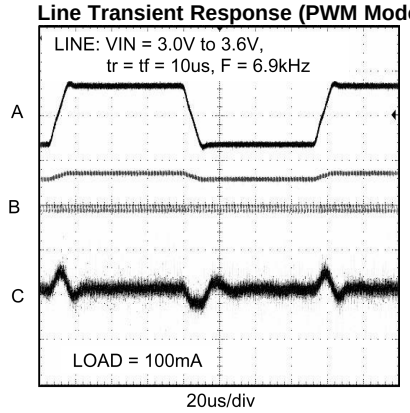
PWM to PFM Response



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 2V/div
C: V_{OUT}, 50mV/div, AC COUPLED
D: SYNC/MODE, 5V/div

Figure 27.

Line Transient Response (PWM Mode)



A: SUPPLY VOLTAGE, 500mV/div, AC COUPLED
B: SW PIN, 5V/div
C: V_{OUT}, 10mV/div, AC COUPLED
L_1 = 22 µH

Figure 28.

DEVICE INFORMATION

The LM2612 is a simple, step-down DC-DC converter optimized for powering low-voltage CPUs or DSPs in cell phones and other miniature battery powered devices. It provides pin-selectable output voltages of 1.05V, 1.3V, 1.5V or 1.8V from a single 2.8V to 5.5V LiION battery cell. It is designed for a maximum load current of 400mA (300mA for B grade).

The device has all three of the pin-selectable operating modes required for cell phones and other complex portable devices. Such applications typically spend a small portion of their time operating at full power. During full power operation, synchronized or fixed-frequency PWM mode offers full output current capability while minimizing interference to sensitive IF and data acquisition circuits. PWM mode uses synchronous rectification for high efficiency: typically 91% for a 100mA load with 1.8V output, 2.8V input. These applications spend the remainder of their time in low-current standby operation or shutdown to conserve battery power. During standby operation, hysteretic PFM mode reduces quiescent current to 160µA typ to maximize battery life. Shutdown mode turns the device off and reduces battery consumption to 0.02µA (typ.).

The LM2612 offers good performance and a full set of features. It is based on a current-mode switching buck architecture. The SYNC/MODE input accepts an external clock between 500kHz and 1MHz. The output voltage selection pins eliminate external feedback resistors. Additional features include soft-start, current overload protection, over-voltage protection and thermal shutdown protection.

The LM2612 is constructed using a chip-scale 10-pin DSBGA package. The DSBGA package offers the smallest possible size for space critical applications, such as cell phones. Required external components are only a small 10uH inductor, and tiny 10uF and 22uF ceramic capacitors for reduced board area.

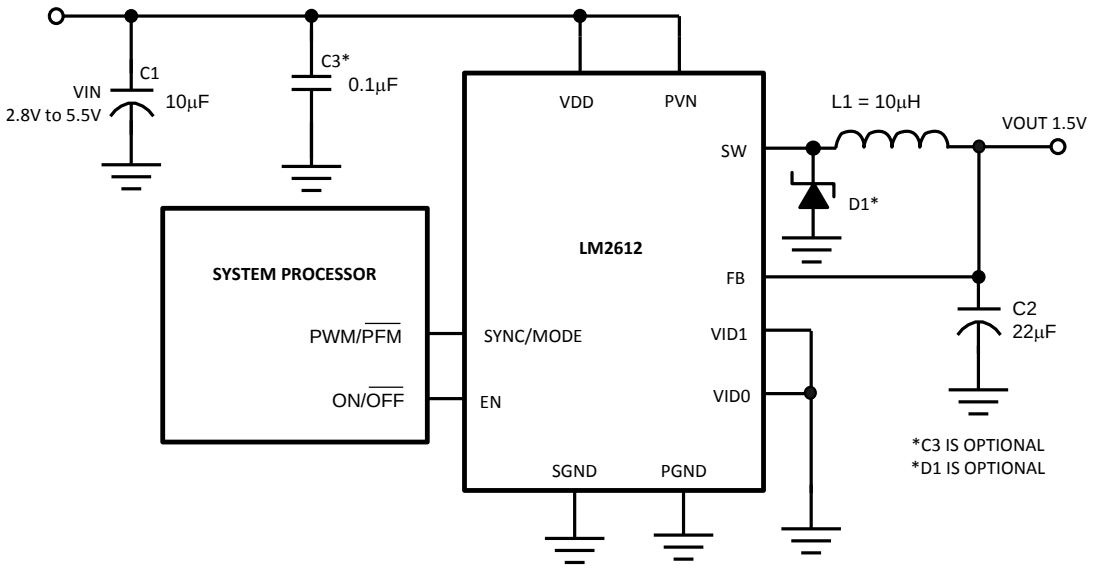


Figure 29. Typical Operating Circuit

Circuit Operation

Referring to Figure 29, Figure 30, and Figure 31, the LM2612 operates as follows: During the first part of each switching cycle, the control block in the LM2612 turns on the internal PFET switch. This allows current to flow from the input through the inductor to the output filter capacitor and load. The inductor limits the current to a ramp with a slope of $(V_{IN} - V_{OUT})/L$, by storing energy in a magnetic field. During the second part of each cycle, the controller turns the PFET switch off, blocking current flow from the input, and then turns the NFET synchronous rectifier on. In response, the inductor's magnetic field collapses, generating a voltage that forces current from ground through the synchronous rectifier to the output filter capacitor and load. As the stored energy is transferred back into the circuit and depleted, the inductor current ramps down with a slope of V_{OUT}/L. If the inductor current reaches zero before the next cycle, the synchronous rectifier is turned off to prevent current reversal. The output filter capacitor stores charge when the inductor current is high, and releases it when low, smoothing the voltage across the load.

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The output voltage is regulated by modulating the PFET switch on-time to control the average current sent to the load. The effect is identical to sending a duty-cycle modulated rectangular wave formed by the switch and synchronous rectifier to a low-pass filter created by the inductor and output filter capacitor. The output voltage is equal to the average voltage at the SW pin.

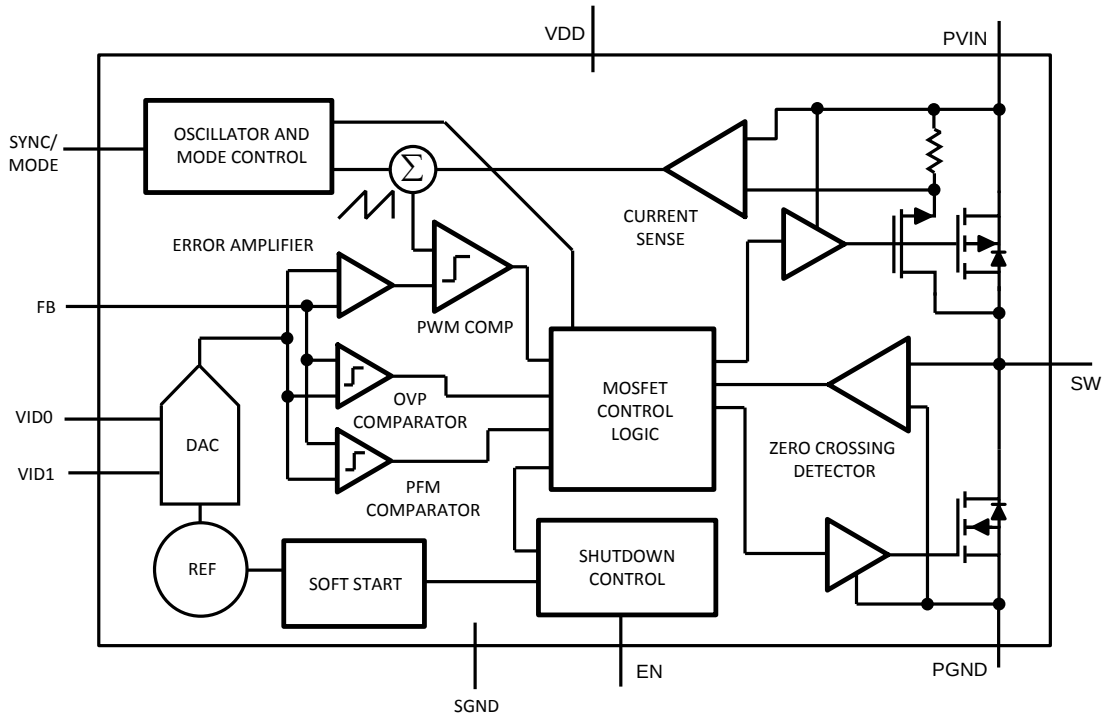


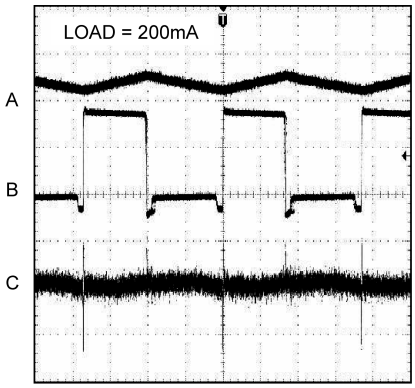
Figure 30. Simplified Functional Diagram

PWM Operation

The LM2612 can be set to current-mode PWM operation by connecting the SYNC/MODE pin to VDD. While in PWM (Pulse Width Modulation) mode, the output voltage is regulated by switching at a constant frequency and then modulating the energy per cycle to control power to the load. Energy per cycle is set by modulating the PFET switch on-time pulse-width to control the peak inductor current. This is done by controlling the PFET switch using a flip-flop driven by an oscillator and a comparator that compares a ramp from the current-sense amplifier with an error signal from a voltage-feedback error amplifier. At the beginning of each cycle, the oscillator sets the flip-flop and turns on the PFET switch, causing the inductor current to ramp up. When the current sense signal ramps past the error amplifier signal, the PWM comparator resets the flip-flop and turns off the PFET switch, ending the first part of the cycle. The NFET synchronous rectifier turns on until the next clock pulse or the inductor current ramps to zero. If an increase in load pulls the output voltage down, the error amplifier output increases, which allows the inductor current to ramp higher before the comparator turns off the PFET switch. This increases the average current sent to the output and adjusts for the increase in the load.

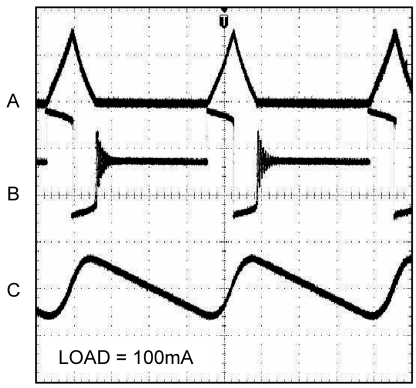
Before going to the PWM comparator, the current sense signal is summed with a slope compensation ramp from the oscillator for stability of the current feedback loop. During the second part of the cycle, a zero crossing detector turns off the NFET synchronous rectifier if the inductor current ramps to zero.

PWM Mode Switching Waveform



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 2V/div
C: V_{OUT}, 10mV/div, AC COUPLED

PFM Mode Switching Waveform



A: INDUCTOR CURRENT, 500mA/div
B: SW PIN, 2V/div
C: V_{OUT}, 50mV/div, AC COUPLED

Figure 31. Typical Circuit Waveforms in (a) PWM Mode and (b) PFM Mode

PFM Operation

Connecting the SYNC/MODE pin to SGND sets the LM2612 to hysteretic PFM operation. While in PFM (Pulse Frequency Modulation) mode, the output voltage is regulated by switching with a discrete energy per cycle and then modulating the cycle rate, or frequency, to control power to the load. This is done by using an error comparator to sense the output voltage and control the PFET switch. The device waits as the load discharges the output filter capacitor, until the output voltage drops below the lower threshold of the PFM error-comparator. Then the error comparator initiates a cycle by turning on the PFET switch. This allows current to flow from the input, through the inductor to the output, charging the output filter capacitor. The PFET switch is turned off when the output voltage rises above the regulation threshold of the PFM error comparator. After the PFET switch turns off, the output voltage rises a little higher as the inductor transfers stored energy to the output capacitor by pushing current into the output capacitor. Thus, the output voltage ripple in PFM mode is proportional to the hysteresis of the error comparator and the inductor current.

In PFM mode, the device only switches as needed to service the load. This lowers current consumption by reducing power consumed during the switching action in the circuit due to transition losses in the internal MOSFETs, gate drive currents, eddy current losses in the inductor, etc. It also improves light-load voltage regulation. During the second part of the cycle, the intrinsic body diode of the NFET synchronous rectifier conducts until the inductor current ramps to zero. The LM2612 does not turn on the synchronous rectifier while in PFM mode.

Operating Mode Selection (SYNC/MODE Pin)

The SYNC/MODE digital input pin is used to select between PWM or PFM operating modes. Set SYNC/MODE high (above 1.3V) for 600kHz PWM operation when the system is active and the load is above 50mA. Set SYNC/MODE low (below 0.4V) to select PFM mode when the load is less than 50mA for precise regulation and reduced current consumption when the system is in standby. The LM2612 has an over-voltage protection feature that may activate if the device is left in PWM mode under low-load conditions (<50mA) to prevent the output voltage from rising too high. See *Overvoltage Protection*, for more information.

Select modes with the SYNC/MODE pin using a signal with a slew rate faster than 5V/100µs. Use a comparator Schmitt trigger or logic gate to drive the SYNC/MODE pin. Do not leave the pin floating or allow it to linger between logic levels. These measures will prevent output voltage errors that could otherwise occur in response to an indeterminate logic state.

Ensure a minimum load to keep the output voltage in regulation when switching modes frequently. The minimum load requirement varies depending on the mode change frequency. A typical load of 8µA is required when modes are changed at 100 ms intervals, 85µA for 10 ms and 800µA for 1 ms.

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Frequency Synchronization (SYNC/MODE Pin)

The SYNC/MODE input can also be used for frequency synchronization. To synchronize the LM2612 to an external clock, supply a digital signal to the SYNC/MODE pin with a voltage swing exceeding 0.4V to 1.3V. During synchronization, the LM2612 initiates cycles on the rising edge of the clock. When synchronized to an external clock, it operates in PWM mode. The device can synchronize to an external clock over frequencies from 500kHz to 1MHz.

Use the following waveform and duty-cycle guidelines when applying an external clock to the SYNC/MODE pin. Each duty cycle between 30% and 70% and the total clock period should be 2µs or less. Clock under/overshoot should be less than 100mV below GND or above V_{DD}. When applying noisy clock signals, especially sharp edged signals from a long cable during evaluation, terminate the cable at its characteristic impedance; add an RC filter to the SYNC pin, if necessary, to soften the slew rate and over/undershoot. Note that sharp edged signals from a pulse or function generator can develop under/overshoot as high as 10V at the end of an improperly terminated cable.

Overvoltage Protection

The LM2612 has an over-voltage comparator that prevents the output voltage from rising too high when the device is left in PWM mode under low-load conditions. Otherwise, the output voltage could rise out of regulation from the minimum energy transferred per cycle due to the 200ns minimum on-time of the PFET switch while in PWM mode. When the output voltage rises by 50mV over its regulation threshold, the OVP comparator inhibits PWM operation to skip pulses until the output voltage returns to the regulation threshold. In over voltage protection, output voltage and ripple increase slightly.

Shutdown Mode

Setting the EN input low to SGND places the LM2612 in a 0.02uA (typ) shutdown mode. During shutdown, the PFET switch, NFET synchronous rectifier, reference, control and bias of the LM2612 are turned off. Setting EN high to VDD enables normal operation. While turning on, soft start is activated.

EN must be set low to turn off the LM2612 during undervoltage conditions when the supply is less than the 2.8V minimum operating voltage. The LM2612 is designed for mobile phones and similar applications where power sequencing is determined by the system controller and internal UVLO (Under Voltage LockOut) circuitry is unnecessary. The LM2612 has no UVLO circuitry. Although the LM2612 exhibits safe behavior while enabled at low input voltages, this is not ensured.

Internal Synchronous Rectification

While in PWM mode, the LM2612 uses an internal NFET as a synchronous rectifier to improve efficiency by reducing rectifier forward voltage drop and associated power loss. In general, synchronous rectification provides a significant improvement in efficiency whenever the output voltage is relatively low compared to the voltage drop across an ordinary rectifier diode.

Under moderate and heavy loads, the internal NFET synchronous rectifier is turned on during the inductor current down-slope in the second part of each cycle. The synchronous rectifier is turned off prior to the next cycle, or when the inductor current ramps near zero at light loads. The NFET is designed to conduct through its intrinsic body diode during transient intervals before it turns on, eliminating the need for an external diode.

Synchronous rectification is disabled and the NFET conducts through its body diode during the second part of each cycle while in PFM mode to reduce quiescent current associated with the synchronous rectifier's control circuitry. To increase efficiency in PFM or PWM conditions, place an external Schottky diode from PGND to SW.

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Current Limiting

A current limit feature allows the LM2612 to protect itself and external components during overload conditions. Current limiting is implemented using an independent internal comparator that trips at current limit of the device. In PWM mode, cycle-by-cycle current limiting is normally used. If an excessive load pulls the output voltage down to approximately 0.7V, then the device switches to a timed current limit mode. In timed current limit mode the internal P-FET switch is turned off after the current comparator trips and the beginning of the next cycle is inhibited for 2.5µs to force the instantaneous inductor current to ramp down to a safe value. PFM mode also uses timed current limit operation. The synchronous rectifier is off in timed current limit mode. Timed current limit prevents the loss of current control seen in some products when the output voltage is pulled low in serious overload conditions.

Current Limiting and PWM Mode Transient Response Considerations

The LM2612 was designed for fast response to moderate load steps. Harsh transient conditions during loads above 300mA can cause the inductor current to swing up to the maximum current limit, resulting in PWM mode jitter or instability from activation of the current limit comparator. To avoid this jitter or instability, do not power-up or start the LM2612 into a full load (loads near or above 400mA). Do not change operating modes or output voltages when operating at a full load. Avoid extremely sharp and wide-ranging load steps to full load, such as from <30mA to >350mA.

Pin Selectable Output Voltage

The LM2612 features pin-selectable output voltage to eliminate the need for external feedback resistors. The output can be set to 1.05V, 1.3V, 1.5V or 1.8V by configuring the VID0 and VID1 pins. See *SETTING THE OUTPUT VOLTAGE* in the *APPLICATION INFORMATION* section for further details.

Soft-Start

The LM2612 has soft start to reduce current inrush during power-up and startup. This reduces stress on the LM2612 and external components. It also reduces startup transients on the power source.

Soft start is implemented by ramping up the internal reference in the LM2612 to gradually increase the output voltage. The reference ramps up in about 400µs. When powering up in PWM mode, soft start may take an additional 200us to allow time for the error amplifier compensation network to charge.

Thermal Shutdown Protection

The LM2612 has thermal shutdown protection that operates to protect from short-term misuse and overload conditions. When the junction temperature exceeds about 150°C, the device shuts down, re-starting in soft start after the temperature drops below 130°C. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

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APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The LM2612 features pin-selectable output voltage to eliminate the need for external feedback resistors. Select an output voltage of 1.05V, 1.3V, 1.5V or 1.8V by configuring the VID0 and VID1 pins, as directed in Table 1.

Table 1. VID0 and VID1 Output Voltage Selection Settings

V_{OUT} (V)	Logic Level	
	VID0	VID1
1.8	0	1
1.5	0	0
1.3	1	0
1.05	1	1

VID0 and VID1 are digital inputs. They may be set high by connecting to VDD or low by connecting to SGND. Optionally, VID0 and VID1 may be driven by digital gates that provide over 1.3V for a high state and less than 0.4V for a low state to ensure valid logic levels. The VID0 and VID1 inputs each have an internal 1.8 µA pull-down that pulls them low for a default 1.5V output when left unconnected. Leaving these pins open is acceptable, but setting the pins high or low is recommended.

INDUCTOR SELECTION

A 10µH inductor with a saturation current rating greater than the max current limit of the device is recommended for most applications. The inductor's resistance should be less than 0.3Ω for good efficiency. Table 2 lists suggested inductors and suppliers.

Table 2. Suggested Inductors and Their Suppliers

Model	Vendor	Phone	FAX
DO1608C-103	Coilcraft	847-639-6400	847-639-1469
DO1606T-103	Coilcraft		
UP1B-100	Coiltronics	561-241-7876	561-241-9339
UP0.4CB-100	Coiltronics		
ELL6GM100M	Panasonic	714-373-7366	714-373-7323
ELL6PM100M	Panasonic		
P1174.103T	Pulse Engineering	858-674-8100	858-674-8262
P0770.103T	Pulse Engineering	858-674-8100	858-674-8262
CDRH5D18-100	Sumida	847-956-0666	847-956-0702
CDRH4D28-100	Sumida		
CDC5D23-100	Sumida		
NP05D B100M	Taiyo Yuden	847-925-0888	847-925-0899
NP04S B100N	Taiyo Yuden		
SLF6025T-100M1R0	TDK	847-803-6100	847-803-6296
SLF6020T-100MR90	TDK		
A918CY-100M	Toko	847-297-0070	847-699-7864
A915AY-100M	Toko		

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For low-cost applications, an unshielded bobbin inductor is suggested. For noise critical applications, a toroidal or shielded-bobbin inductor should be used. A good practice is to lay out the board with overlapping footprints of both types for design flexibility. This allows substitution of a low-noise toroidal inductor, in the event that noise from low-cost bobbin models is unacceptable.

The saturation current rating is the current level beyond which an inductor loses its inductance. Beyond this rating, the inductor loses its ability to limit current through the PFET switch to a ramp and allows the switch current to increase rapidly. This can cause poor efficiency, regulation errors or stress to DC-DC converters like the LM2612. Saturation occurs when the magnetic flux density from current through the windings of the inductor exceeds what the inductor's core material can support with energy storage in a corresponding magnetic field.

Table 3. Suggested Capacitors and Their Suppliers

Model	Size	Vendor	Phone	FAX
22µF, X7R or X5R Ceramic Capacitor for C2 (Output Filter Capacitor)				
C3225X5RIA226M	1210	TDK	847-803-6100	847-803-6296
JMK325BJ226MM	1210	Taiyo-Yuden	847-925-0888	847-925-0899
ECJ4YB0J226M	1210	Panasonic	714-373-7366	714-373-7323
GRM42-2X5R226K6.3	1210	muRata	404-436-1300	404-436-3030
10µF, 6.3V, X7R or X5R Ceramic Capacitor for C1 (Input Filter Capacitor)				
C2012X5R0J106M	0805	TDK	847-803-6100	847-803-6296
JMK212BJ106MG	0805	Taiyo Yuden	847-925-0888	847-925-0899
ECJ3YB0J106K	1206	Panasonic	714-373-7366	714-373-7323
GRM40X5R106K6.3	0805	muRata	404-436-1400	404-436-3030

CAPACITOR SELECTION

Use a 10µF, 6.3V, X7R or X5R ceramic input filter capacitor and a 22uF, X7R or X5R ceramic output filter capacitor. These provide an optimal balance between small size, cost, reliability and performance. Do not use Y5V ceramic capacitors. Table 3 lists suggested capacitors and suppliers.

A 10µF ceramic capacitor can be used for the output filter capacitor for smaller size in applications where the worst-case transient load step is less than 200mA. Use of a 10µF output capacitor trades off smaller size for an increase in output voltage ripple, and undershoot during line and load transient response.

The input filter capacitor supplies current to the PFET switch of the LM2612 in the first part of each cycle and reduces voltage ripple imposed on the input power source. The output filter capacitor smoothes out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficient capacitance and sufficiently low ESR to perform these functions.

The ESR, or equivalent series resistance, of the filter capacitors is a major factor in voltage ripple. The contribution from ESR to voltage ripple is around 75-95% for most electrolytic capacitors and considerably less for ceramic capacitors. The remainder of the ripple is from charge storage due to capacitance.

DIODE SELECTION

An optional Schottky diode (D1 in Figure 1) can be added to increase efficiency in PFM mode and PWM mode. This may be desired in applications where increased efficiency for improving operational battery life takes precedence over increased system size associated with the Schottky diode. Typically, use of an external schottky diode increases PFM mode efficiency from 72.7% to 85.0% (20 mA load, V_{OUT} = 1.8V, V_{IN} = 3.6V). See the efficiency curves in the *TYPICAL OPERATING CHARACTERISTICS*.

Use a Schottky diode with a current rating higher than maximum current limit, such as an MBRM120T3 or MBRM140T3. Use of a device rated for 30V or more reduces diode reverse leakage in high temperature applications

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DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful reflow techniques, as detailed in Application Note AN-1112, *AN-1112 DSBGA Wafer Level Chip Scale Package* (literature number SNVA009). Refer to the section *Surface Mount Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. Since DSBGA packaging is a new technology, all layouts and assembly means must be thoroughly tested prior to production. In particular, proper placement, solder reflow and resistance to thermal cycling must be verified.

The 10-Bump package used for the LM2612 has 300micron solder balls and requires 10.82mil (0.275mm) pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 6 mil wide, for a section 6 mil long or longer, as a thermal relief. Then each trace should neck up to its optimal width over a span of 11 mils or more, so that the taper extends beyond the edge of the package. The important criterion is symmetry. This ensures the solder bumps on the LM2612 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3, B3, C3, D3 and A2. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal reliefs can result in late or inadequate reflow of these bumps.

The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size or 14.7mils for the LM2612. This prevents a lip that otherwise forms if the solder-mask and pad overlap. This lip can hold the device off the surface of the board and interfere with mounting. See Applications Note AN-1112 (SNVA009) for specific instructions.

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BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces. These can send erroneous signals to the DC-DC converter IC, resulting in poor regulation or instability. Poor layout can also result in reflow problems leading to poor solder joints between the DSBGA package and board pads. Poor solder joints can result in erratic or degraded performance.

Good layout for the LM2612 can be implemented by following a few simple design rules:

1. Place the LM2612 on 10.82mil pads for DSBGA package. As a thermal relief, connect to each pad with a 6mil wide trace (DSBGA), 6mils long or longer, then incrementally increase each trace to its optimal width over a span so that the taper extends beyond the edge of the package. The important criterion is symmetry, to ensure re-flow occurs evenly (see *DSBGA PACKAGE ASSEMBLY AND USE*).
2. Place the LM2612, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Place the capacitors and inductor within 0.2in (5mm) of the LM2612.
3. Arrange the components so that the switching current loops curl in the same direction. During the first part of each cycle, current flows from the input filter capacitor, through the LM2612 and inductor to the output filter capacitor and back through ground, forming a current loop. In the second part of each cycle, current is pulled up from ground, through the LM2612 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Routing these loops so the current curls in the same direction prevents magnetic field reversal between the two part-cycles and reduces radiated noise.
4. Connect the ground pins of the LM2612 and filter capacitors together using generous component-side copper fill as a pseudo-ground plane. Then, connect this to the ground-plane with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It is recommended to have a dedicate ground plan between the switch signal and feedback traces. It also reduces ground bounce at the LM2612 by giving it a low-impedance ground connection.
5. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
6. Route noise sensitive traces, such as the voltage feedback path, away from noisy traces between the power components. The voltage feedback trace must remain close to the LM2612 circuit and should be direct but routed away from noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
7. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter in one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages in the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators, such as the LP2966.

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REVISION HISTORY

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	18

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